CLAIMS

What is claimed is:

1. A method comprising:

dynamically modifying one or more attributes of each of a plurality of requests to access one or more memory devices; and

arbitrating among the plurality of requests to select a request to send to the one or more memory devices in a time slot based on the one or more attributes.

2. The method of claim 1, wherein dynamically modifying the one or more attributes comprises dynamically prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests.

3. The method of claim 2, wherein the latency sensitivity of each of the plurality of requests changes in response to space available in a buffer storing the corresponding request.

4. The method of claim 1, further comprising dynamically changing a length of each of the plurality of requests in response to a size of the time slot.

5. The method of claim 1, wherein the plurality of requests comprises one or more data read requests, one or more data write requests, and one or more buffer descriptor read requests.

6. The method of claim 1, further comprising sending the selected request to the memory devices via a digital multimedia interconnect.

7. The method of claim 1, further comprising asserting the plurality of requests using a plurality of direct memory access (DMA) controllers in response to an instruction from a processor.

8. A machine-accessible medium that provides instructions that, if executed by a processor, will cause the processor to perform operations comprising:

arbitrating among a plurality of requests to access one or more memory devices to select a request to send to the one or more memory devices in a time slot based on one or more attributes of the plurality of requests; and

dynamically changing a length of each of the plurality of requests in response to a size of the time slot.

9. The machine-accessible medium of claim 8, wherein the operations further comprise dynamically prioritizing the plurality of requests in response to latency sensitivity of each of the plurality of requests.

10. The machine-accessible medium of claim 9, wherein the latency sensitivity of each of the plurality of requests changes in response to space available in a buffer storing the corresponding request.

11. The machine-accessible medium of claim 8, wherein the plurality of requests comprises one or more data read requests, one or more data write requests, and one or more buffer descriptor read requests.

12. The machine-accessible medium of claim 8, wherein the operations further comprise sending the selected request to the one or more memory devices via a digital multimedia interconnect.

13. An apparatus comprising:

a plurality of memory access controllers to assert a plurality of requests to access memory devices, wherein one or more attributes of the plurality of requests are dynamically changeable; and

a first arbiter to arbitrate among the plurality of requests to select a request based on the one or more attributes of the plurality of requests.

14. The apparatus of claim 13, wherein each of the plurality of memory access controllers further comprises a buffer to temporarily store one or more requests, a priority state machine to dynamically prioritize the one or more requests, and request length determination circuitry to determine length of the one or more requests.

15. The apparatus of claim 14, wherein the request length determination circuitry comprises a plurality of multiplexers.

16. The apparatus of claim 15, wherein the request length determination circuitry further comprises one or more flip-flops coupled to the plurality of multiplexers.

17. The apparatus of claim 13, wherein the first arbiter comprises a first plurality of arbiters and a second arbiter, outputs of the first plurality of arbiters are coupled to inputs of the second arbiter.

18. The apparatus of claim 17, wherein the first plurality of arbiters comprise a plurality of First Come First Serve (FCFS) arbiters.

19. The apparatus of claim 17, wherein the second arbiter comprises a fixed priority arbiter.

20. The apparatus of claim 14, wherein the priority state machine prioritizes the plurality of requests based on space available in the buffer of each of the plurality of memory access controllers.

21. A system comprising:

a plurality of dynamic random access memory (DRAM) devices;

one or more audio coder-decoders; and

an input/output controller, coupled between the DRAM devices and the one or more audio coder-decoders, the input/output controller having an audio controller, the audio controller comprising

a plurality of memory access controllers to assert a plurality of requests to access one or more of the DRAM devices, wherein one or more attributes of the plurality of requests are dynamically changeable; and

a first arbiter to arbitrate among the plurality of requests to select a request based on the one or more attributes of the plurality of requests.

22. The system of claim 21, wherein each of the plurality of memory access controllers further comprises a buffer to temporarily store one or more requests, a priority state machine to dynamically prioritize the one or more requests, and request length determination circuitry to determine length of the one or more requests.

23. The system of claim 22, wherein the request length determination circuitry comprises:

a plurality of multiplexers; and

one or more flip-flops coupled to the plurality of multiplexers.

24. The system of claim 21, wherein the first arbiter comprises a first plurality of arbiters and a second arbiter, outputs of the first plurality of arbiters are coupled to inputs of the second arbiter.

25. The system of claim 24, wherein the first plurality of arbiters comprise a plurality of First Come First Serve (FCFS) arbiters.

26. The system of claim 24, wherein the second arbiter comprises a fixed priority arbiter.

27. The system of claim 22, wherein the priority state machine prioritizes the plurality of requests based on space available in the buffer of each of the plurality of memory access controllers.

28. The system of claim 21, further comprising:

a memory controller coupled to the DRAM devices; and

a digital multimedia interconnect, coupled between the memory controller and the input/output controller, wherein the selected request is sent to one or more of the DRAM devices via the digital multimedia interconnect and the memory controller.

29. The system of claim 28, further comprising a central processing unit, coupled to the memory controller, to send an instruction to the input/output controller to cause the plurality of memory access controllers to assert the plurality of requests.